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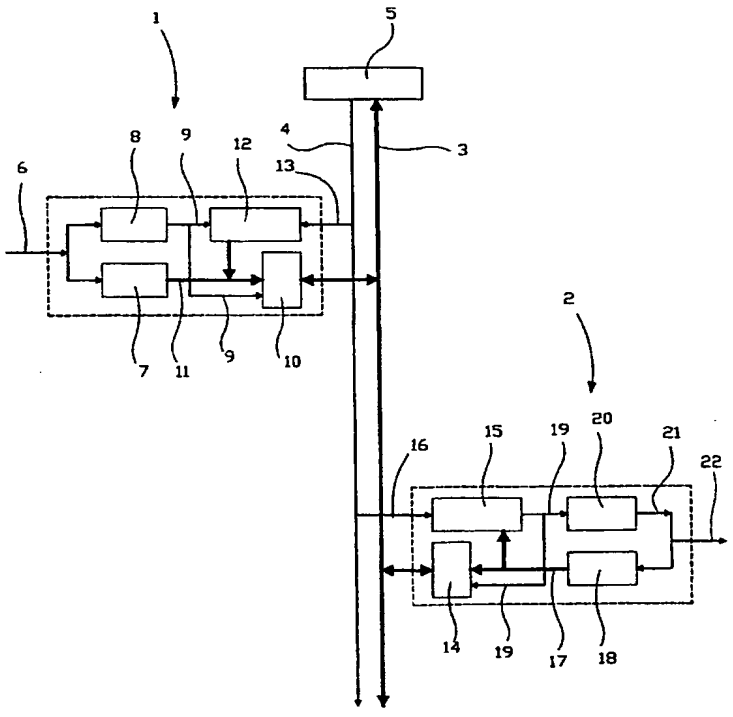
(54) Title: METHOD FOR SYNCHRONIZING CLOCKS IN ELECTRONIC UNITS CONNECTED TO A MULTI PROCESSOR DATA BUS



(57) Abstract: A method and apparatus for synchronizing clocks in a master unit (1) and one or more slave units (2) connected to a multi processor data bus (3) including a bus clock signal (4), where the master unit (1) receives from an external source, or generates locally, a master clock signal to be reproduced on each slave. The master unit (1) repeatedly sends data values representing the current data bus clock (4) frequency, and the elapsed master (1) time to slaves (2) via the data bus (3). Each slave (2) on reception of said data values, establishes a division ratio needed to produce the master (1) clock frequency from the bus clock (4) frequency and applies such a division to the bus clock signal (4). The slave (2) keeps a slave (2) time value in units of the time period in the output signal and compares the slave (2) time to the received master (1) and adjusts the frequency division to compensate for time differences and bring the slave (2) time to equal the master (1) time.

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A protocol known as I_2O allows units connected to a PCI bus to communicate (peer to peer) without involving the main central processor (CPU). The PCI bus then act as a high speed network where all units may initiate data transfer without interrupting the main CPU. Other multi processor protocols exist for different types of multi processor data buses. Utilizing these known multi processor data buses and protocols for real time transmission and processing, would however, require additional dedicated clock signal generators and clock signal lines to implemented.

The object of the present invention is to provide a method and an apparatus for synchronizing clocks on units connected to an ordinary multi processor data bus, thus making a data bus, such as the PCI bus, suitable for real time data transfer.

The object is achieved by means explained in the following description and in the patent claims.

References will be made to the PCI bus, telephone systems and transmission of live sound or video, but the present invention is applicable to all types of multi processor data buses and time critical data.

According to the invention, a process clock signal on a master unit connected to a multiprocessor data bus is reproduced on slave units connected to the data bus by the following method.

The master unit and one or more slave units are connected to a multi processor data bus including a bus clock signal. The master unit receives from an external source, or generates locally, a master clock signal to be reproduced on each slave.

The master unit repeatedly establishes a numeric value representing the ratio between the data bus clock frequency and the frequency of a time base clock signal derived from the master clock signal. It can be seen that the bus clock to base clock frequency ratio represents the bus clock frequency measured in said time base. If the base clock runs at 1 Hz the bus clock to base clock frequency ratio is of course numerically equal to the bus clock frequency in periods per second. The master unit also establishes the current time in master clock time units, typically by counting pulses on the master clock signal.

The master unit repeatedly sends the current time in master clock units and the current bus clock frequency (or bus

clock to base clock frequency ratio) to each slave unit via the data bus.

Each slave unit establishes from the bus clock frequency value received from the master, a suitable division ratio for producing the required slave clock signal frequency from the bus clock frequency. The slave clock frequency may be generated in one or more steps, for example by dividing the bus clock frequency down to a frequency lower than the required slave clock frequency, thereby obtaining a base frequency suitable for a frequency multiplier and a stabilizing phase locked loop circuit.

Each slave unit keeps track of slave clock time by counting clock pulses on the slave clock signal. The slave calculates a time difference by subtracting slave clock time from the master clock time received from the master unit. If there is a non zero time difference, the slave may adjust the frequency division in order to increase or decrease the slave clock frequency to compensate for and catch up with the time difference. The time difference may operate on an integrated time difference for better stability.

There is a time delay between the master and it slaves. At the time when a slave gets around to handle the received values, the master clock is not equal to the value seen by the slave. This can be compensated for by having slaves, or other units, respond to data sent by the master. The master can measure the average response time and calculate an average time delay representing estimate the transmission time from server to slave. This difference can be compensated for by adding a transmission delay to the master time vale before sending it to the slaves.

If the master or a slave drops out for a period, perhaps due to plugging or unplugging communication lines or other equipment, synchronization is effectively lost. Slaves may however, be made quite fault tolerant. If a new master time value is not received within a predefined time period, the slave continues producing the slave clock signal and counting slave clock pulses. The time difference is however, not corrected for. If the master comes back on line and a slave receives a master time value that differs from the slave time by

more than a predefined value, typically a fraction of a second, the slave will set its slave time equal to the received master time, clear the time difference register and resume normal operation. The master can of course

alternatively emit a reset clock command to all slaves when it comes on line.

If a slave drops out and comes back on line, the slave will set its slave time equal to the first master time value received, clear the time difference register and start normal operation.

The slave unit will typically apply an integer division to the bus clock frequency to reproduce the master clock frequency. This will seldom be accurate, and the slave will apply a divisor that is one unit too low part of the time and too high part of the time to get a correct average.

If a 33 MHz bus clock is off by +23 parts per million, bus clock runs 33.000759 MHz. To produce a 8 kHz frequency, the 33.000759 MHz signal must be divided by 4125.094875 as opposed to 4125 if the bus clock was accurate. If an integer divisor was applied 8000 times during one second, a divisor value of 4126 applied 759 times and 4125 applied 7241 times would produce the exact 8 kHz from the 33.000759 MHz. To prevent jitter in the resulting clock signal when changing the divisor, a slow settling (1 second or more) phase locked loop circuit will provide smooth transitions. Also, the 759 instances of divisor 4126 should be distributed evenly over the 8000 divisions, thus every tenth or eleventh division should use the value 4126.

An apparatus for applying the said method will be described by means of an example with reference to the attached drawing where reference numeral 1 designates a master unit indicated by a dashed rectangle and 2 is a slave unit also indicated by a dotted rectangle.

The master 1 and slave 2 are connected to a multi processor data bus 3 comprising a bus clock line 4 carrying a bus clock signal controlled by a bus master circuit 5.

A master clock signal from a source not shown, is fed to the master 1 via a clock input 6 and split to a an incrementing counter 7 and dividing counter 8 set to divide the incoming signal with a predefined value. The dividing counter 8 is by this example set to divide the master clock signal frequency to produce a 1 Hz time base signal at the output 9. The time base signal is fed to a microprocessor 10, preferable to an interrupt input so that the microprocessor 10 can promptly respond to the time base signal, here once a second.

The microprocessor 10 is connected to the the incrementing counter 7 by a local bus 11 and can read the counter 7

value from its counting register. The value of the incrementing counter 7 represents the master time in master clock signal time units. The microprocessor 10 is also connected to the data bus 3 as an ordinary peripheral unit and can exchange data with other units connected to the data bus 3. The microprocessor 10 is, via the local bus 11, connected to a frequency counter 12 and is thereby able to read its counting register. The count signal input 13 of counter 12 is connected to the bus clock line 4.

The microprocessor reads the counting register in the counter 12 periodically at a rate set by the signal output 9 of the dividing counter 8, in this example every second. The count register value or the change in the count register value of counter 12, depending on the counter type chosen for the design, represents the number of bus clock 4 pulses counted in one base time period, in this example pulses per second or the bus clock frequency. The microprocessor also reads the counting register of the ncrementing counter 7 representing the current master time, which may be the time elapsed since system startup in master clock time units. The microprocessor emits the bus clock 4 frequency value as read from counter 12 and the current master time value as read from counter 7 on the data bus 3 while at the same time addressing one or more slave units connected to the bus 3, 4. The address bus is not shown. The operation is repeated for every base time signal on output 9 from counter 8.

The slave unit 2 is has a microprocessor 14 connected to the data bus 3 capable communicating with other units connected to the data bus 3,4, in particular receiving information from the master unit 1.

A programmable counter 15 has its count input line 16 connected to the clock line 4. The microprocessor 14 is connected to the programmable counter 15 by a local bus 17 which is also connected to an integrating counter 18. The microprocessor 14 can via the bus 17 write to the counter register in the programmable counter 15 and read the counting register in the incrementing counter 18. The programmable counter 15 counts clock pulses on the bus clock line 4. When a number of clock pulses preprogrammed by the microprocessor 14, have been reached, the counter 15 emits a pulse on its output 19 and starts a new count sequence. The time measured elapsing between successive pulses emitted

on counter 15 output 19, canbe is preset by the writing a value corresponding to a number of bus clock 4 pulses in

counter 15. Also, the output 19 is connected to the microprocessor 14, preferably to an interrupt input. The microprocessor 14 will respond to pulses emitted by counter 15 and update its counter register to produce the correct frequency.

The output 19 is connected to the input of a frequency signal generator 20 that on its output 21 will produce a frequency depending on the frequency of the pulses emitted by the programmable counter 15. The frequency generator output signal also appears on the output of the slave 2. Thus the output frequency of the signal generator 20 is controllable by values written to the counting register of counter 15. The output of signal generator 20 is kept synchronized with the master clock signal fed to the master 1 input 6 by the method according to the invention. The signal generator 20 output 21 is connected to the signal input of the incrementing counter 18. The content of counter 18 represents slave 2 time in time units determined by the frequency out-putted from the signal generator 20. The microprocessor will adjust the counting register in the programmable counter 15 to keep the slave 2 time equal to the master 1 time. The frequency controlled signal generator 20 is preferably a phase locked loop circuit. Since the wanted output signal frequency is fixed, the signal generator 20 will receive a fairly constant frequency input signal from counter 15.

The bus clock frequency value and the master 1 clock value transmitted on the data bus by the master 1, are received by the microprocessor 14 in the slave 2. The bus clock frequency value is in this example divided by a factor required to make counter 15 emit pulses at a rate that will make the generator 20 produce the correct frequency. The master 1 time value is compared with the slave 2 time vale read from counter 18. If there is a time difference, the difference value, which may be positive or negative, is integrated in the microprocessor and

used to adjust the count value written to counter 15 to make the slave 1 time catch up and synchronize with the master 1 time.

Claims

1. A method for synchronizing clocks in a master unit (1) and one or more slave units (2) connected to a multi processor data bus (3) including a bus clock signal (4), where the master unit (1) receives on an input (6) from an external source, or generates locally, a master clock signal to be reproduced on an output (22) of each slave, characterized in that the master unit (1) repeatedly sends data values representing the current data bus clock (4) frequency and the elapsed master (1) time to slaves (2) via the data bus (3), and in that each slave (2) on reception of said data values, establishes a division ratio needed to produce the master (1) clock frequency from the bus clock (4) frequency and applies such a division to the bus clock signal (4).

2. A method according to claim 1, characterized in that the slave (2) keeps a slave (2) time value in units of the time period in the output signal and compares the slave (2) time to the received master (1) and adjusts the frequency division to compensate for time differences and bring the slave (2) time to equal the master (1) time.

3. An apparatus for synchronizing clocks in a master unit (1) and one or more slave units (2) according to claim 1 or 2, characterized in that the master (1) comprises an incrementing counter (7) and a dividing counter (8) having their count input connected to the master (1) clock signal and the output of the dividing counter (8) is connected to the time base input of a frequency counter (12) which has its count input connected to the bus clock (4) signal, and where the count register of the incrementing counter (7) and the frequency counter (12) is readable by a microprocessor (10) cconnected to the data bus (3)

4. An apparatus for synchronizing clocks in a master unit (1) and one or more slave units (2) according to claim 1 or 2, characterized in that the slave (2) comprises a programmable counter (15) having its count input connected to the bus clock line (4) and its count output signal connected to the input of a frequency controlled frequency signal generator (20), and a microprocessor (14) connected to the data bus (3) is connected to counter (15) and capable of writing count values into the counter (15), and that the output of the signal generator (20) is connected to the input of an incrementing counter (18) having its count register

readable by the microprocessor (14), which is also connected to and able to react on the output signal (19) from the programmable counter (20).

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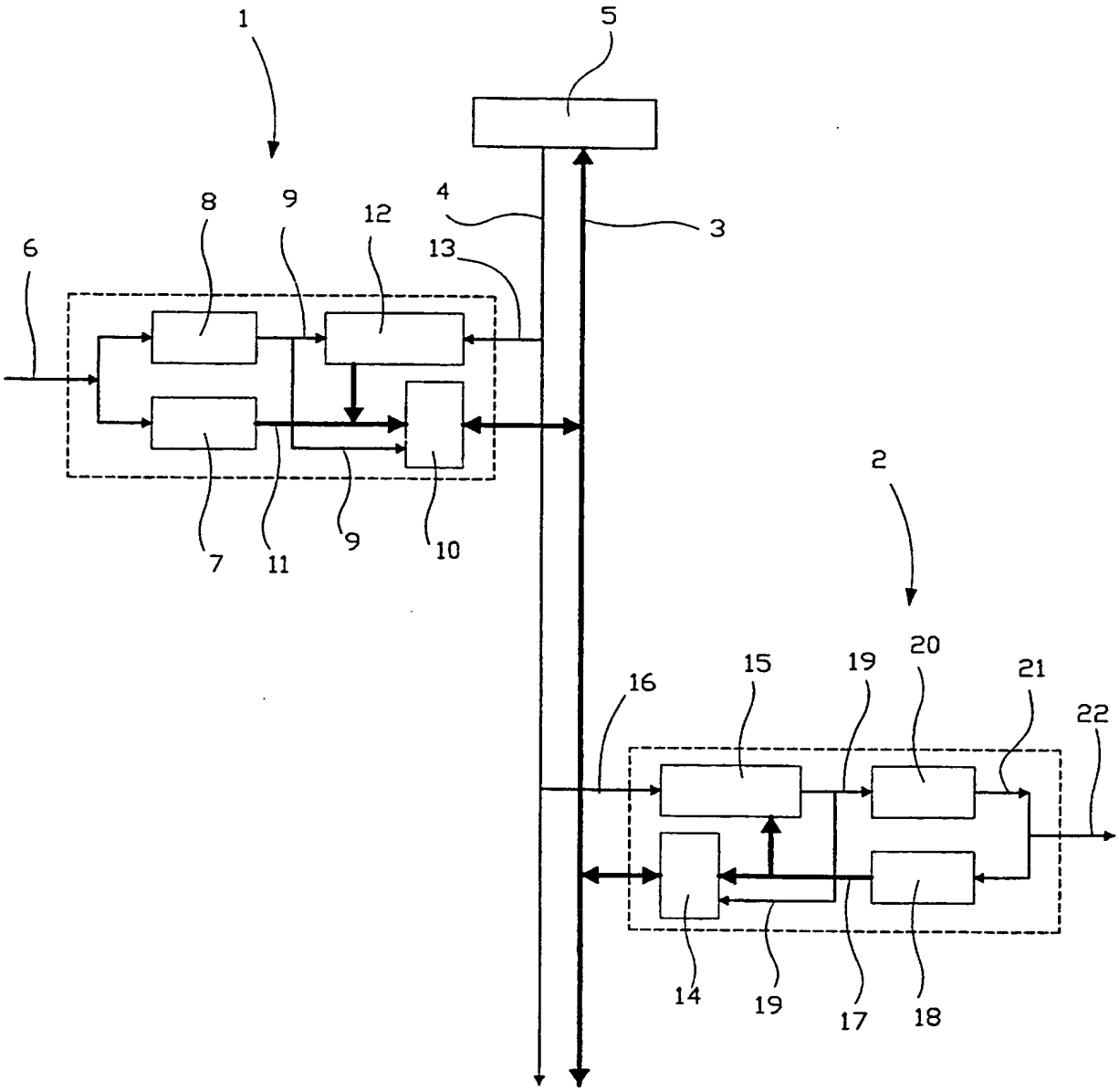

FIG. 1

INTERNATIONAL SEARCH REPORT

International application No.
PCT/NO 99/00290

A. CLASSIFICATION OF SUBJECT MATTER

IPC7: G06F 1/12
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC7: G06F

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

SE,DK,FI,NO classes as above

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
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A	US 4882739 A (RICHARD J. POTASH ET AL), 21 November 1989 (21.11.89), abstract ---	1-4
A	JP7281785 A (TOSHIBA KK) 1995-10-27 (abstract) World Patents Index [online]. London, U.K.: Derwent Publications, Ltd. [retrived on 2000-06-22] Retrived from: EPO WPI Database. DW199601 Accession No.1996-004830 JP 7281785 (TOSHIBA KK)1996-02-29 (abstract)[online][retrived on 2000-06-22] Retrived from: EPO PAJ Database; JP 07-281785 (TOSHIBA KK) 27 October 1995 ---	1-4

[X] Further documents are listed in the continuation of Box C. [X] See patent family annex.

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Date of the actual completion of the international search	Date of mailing of the international search report
22 June 2000	07 JUL 2000
Name and mailing address of the ISA/ Swedish Patent Office Box 5055, S-102 42 STOCKHOLM Facsimile No. +46 8 666 02 86	Authorized officer Håkan Sandh/mj Telephone No. +46 8 782 25 00

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INTERNATIONAL SEARCH REPORT

International application No.
PCT/NO 99/00290

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 5327468 A (WARREN A. EDBLAD ET AL), 5 July 1994 (05.07.94), abstract -- --------	1-4

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INTERNATIONAL SEARCH REPORT

Information on patent family members

02/12/99

International application No.
PCT/NO 99/00290

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